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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/732,730	12/10/2003	Rui M. Bastos	NVDA P000573	6695

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EXAMINER	
TUNG, KEE M	

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/732,730	BASTOS ET AL.	
	Examiner	Art Unit	
	Kee M. Tung	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-7,9-12,16 and 21-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7,9-12,16,21,24 and 26-29* is/are rejected.

7)☒ Claim(s) *22,23 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed 7/25/05 has been considered in preparing this Office action.

Claim Rejections - 35 USC § 112

2. Claim 25 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 25, line 4, "the processor" is unclear to which processor is being referred to, the graphics processor or the fragment processing unit.

3. Claim 24 recites the limitation "the fragment processing unit" in line 3. There is insufficient antecedent basis for this limitation in the claim.

4. Claim 28 recites the limitation "the displaced meshes" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 5-7, 9-12, 24, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gannett (6,118,452).

Gannett teaches a graphics processor (Fig. 1A, 116) configured to produce data for multiple output buffers (col. 8, lines 61-67, respective buffers in the frame buffer

232), each output buffer associated with a unique output buffer identifier (not explicitly teach or suggest by Gannett, however, Gannett teaches "drawn into an **appropriate** frame buffer" (col. 8, lines 4-7); and "respective **buffers** in the frame buffer 232, include a color buffer, depth buffer, accumulation buffer and stencil buffer" (col. 8, lines 61-67). Gannett further teaches the fragment processing pipeline determines an address associated with the processed fragment data, the address corresponding to a specific location in an output buffer (obvious by the teachings of "drawn into an appropriate frame buffer" (col. 8, lines 4-7) and "respective buffer" (col. 8, line 64)). It would have been obvious to one of ordinary skill in the art at the time the present invention was made that a buffer identifier would have been obvious in order for each of the fragment operation stages to store or identifier their respective buffer in more efficient and effective manner and thus to improve the system performance.), comprising a fragment processing pipeline (168) configured to process graphics data to produce processed graphics data for the multiple output buffers and determine at least one output buffer identifier associated with the processed graphics data; a shader read interface (frame buffer controller in side the frame buffer and control 170) configured to read processed graphics data associated with an output buffer identifier from an output buffer stored in a memory; and a write interface (also by the frame buffer controller which controls both read from and write to the frame buffer) configured to write processed graphics data associated with at least one output identifier to an output buffer stored in the memory. Therefore, at least claims 1 and 9 would have been obvious.

As per claim 2, Gannett fails to explicitly suggest or teach a geometry processor configured to process graphics data. However, as well known in the graphics art, a graphics subsystem (or processor or controller) includes a front end processor which is called geometry processor and a back end subsystem (or processor or controller) is called rasterizer or renderer. Therefore, the teaching of geometry processor is an inherent in view of the teachings of graphics processor of Gannett.

As per claim 3, Gannett teaches at least one output buffer identifier is determined by a fragment program executed in the fragment processing pipeline (such as, the one of the fragment modules in Fig. 20.

As per claim 5, Gannett teaches the output buffer identifier is readable and writable by the fragment processing pipeline (enable each fragment operation stage to store their respective data into its buffer).

As per claim 6, Gannett teaches any of the multiple output buffers is selected for display using the address defined in the fragment processing pipeline (abstract and further see claim 1 above).

As per claim 7, Gannett fails to explicitly teach or suggest the fragment processing pipeline includes multiple registers, each register capable of outputting data to one or more of the multiple output buffers. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the teachings of fragment operation stages of Gannett because a register (or a buffer) is a temporary storage device for storing data between components in order to over come idol time when the next stage is not readily to accept the data.

Claims 10 and 11 are similar in broader scope than claim 1, and thus are rejected under similar rationale.

As per claim 12, Gannett teaches the processed fragment data stored in the output buffer includes fragment depth data (col. 8, lines 65 and 66).

As per claim 15, Gannett fails to explicitly teach or suggest the index is a pointer to a fragment program. It would have been obvious to one of ordinary skill in the art at the time the present invention was made that the feature would have been obvious in view of the teachings of well known and well used OpenGL specification in the computer graphics art.

As per claim 24, Gannett teaches the fragment processing pipeline is configured to process the graphics data of at least two fragments in parallel, the fragment processing unit determining the destination address in one of the output buffers for each of the fragments (pipeline processing is considered one particular type of parallel processing in any time, there are at least two stages processing two fragments in parallel from two different stages of the pipeline).

As per claims 26 and 27, Gannett teaches the fragment processing pipeline is configured to process graphics data to produce visible fragment data for visible fragment (222 and Fig. 3); one of multiple output buffers stored depth map values of the visible fragments (depth buffer); one or more of the output buffers store fragment data (232); a shader (col. 7, line 60) for shading the visible fragments using the portion of the fragment data read from the one or more of the output buffers and the depth map read one of the output buffers.

7. Claims 4 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gannett (6,118,452) in view of Airey et al (6,650,327 hereinafter "Airey").

The teachings of Gannett are given in previous paragraph of this Office action. Gannett further teaches an output buffer includes data represented in two or more data formats (such as, different formats for pixel color for color buffer and depth value for Z-buffer). However, Gannett fails to explicitly teach or suggest the data formats includes fixed point and floating point or including different number of bits within the same output buffer. Airey teaches a frame buffer (140) can be used to store floating point data format in different number of bits. Airey further teaches there are many different advantages to store or process graphics data in floating point format than the prior art fixed point format. However, the frame buffer can still be used to store fixed point format data. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Airey into the system of Gannett in order to obtain all the advantages as taught by Airey (col. 2, lines 10-28 and lines 58-67; col. 3, lines 3-67; col. 8, lines 42-67, col. 9, lines 1-9 and many other areas of the specification). Therefore, at least claims 4 and 21 would have been obvious.

8. Claims 16, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gannett (6,118,452) in view of Mori et al (6,704,018 hereinafter "Mori").

The teachings of Gannett are given in previous paragraph of this Office action. However, Gannett fails to explicitly teach or suggest the processed fragment data stored in the output buffer includes displaced mesh data, the method including

displacing the processed fragment data to produce one or more displaced meshes, and storing each of the displaced meshes in one of the multiple output buffers. This is what Mori teaches (Fig. 9). Mori further teaches a computer graphics system (Fig. 1) comprising a graphics processor (Fig. 2, 8) includes vertex processor (30), a cache (70), a frame memory access unit (50), rendering processor (40), and a frame memory (80). The frame memory (Fig. 3) further includes multiple buffers (801-806). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Mori into the system of Gannett in order to draw high quality 3D compute graphics in real time as taught by Mori (col. 1, lines 13-15). Therefore, at least claim 16 would have been obvious.

As per claim 28, Mori teaches each of the displaced meshes is used as a vertex array to animated geometry (Fig. 9 and col. 2, lines 30-34).

As per claim 29, Mori teaches displacing the processed fragment data along a normal vector to produce the displaced meshes (Fig. 9, S204).

Response to Arguments

9. Applicant's arguments filed 7/25/05 have been fully considered but they are not persuasive.

Regarding amended claim 1, applicant argues that Gannett fails to suggest or teach, an output buffer identifier associated with the processed graphics data. The examiner disagrees. As stated above in the detailed rejection, Gannett teaches multiple output buffers, such as, depth, color, accumulation and stencil buffers (col. 8, lines 65-67) for storing the different data. If there is no "unique buffer identifier" to distinguish the

different buffers, the different data may stored into wrong buffers, for example, depth data may stored in color buffer and color data may stored in the depth buffer. Therefore, the output buffer identifier is considered obvious by the teachings of multiple buffers of Gannett.

Regarding claim 4, a new prior art has been incorporated into the rejection.

Regarding claim 6, it is noted that it was old and well known in the art that the display data is read out from the output buffer in accordance with the address location specify by the buffer controller and displaying on the display screen. The abstract teaches "enables the graphics system to selectively perform graphics pipeline operations which are related to pixels which are ultimately displayed on the display".

Regarding claim 26, applicant argues that "the ability to avoid display of invisible fragments by displaying and calculating only visible fragments is achieved as claimed in claim 26 but is not found in Gannett." The examiner disagrees. Gannett clearly teaches the claimed feature and this is also what Gannett tries to achieve (see abstract, "the processing associated with performing operations on non-displayed pixels is avoided thereby providing the graphics system with signification performance enhancement").

Regarding claims 16, 27 and 29, Mori teaches the claimed features as discussed in detail rejection above.

Allowable Subject Matter

10. Claims 22, 23 and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kee M. Tung whose telephone number is 571-272-7794. The examiner can normally be reached on Tuesday - Friday from 5:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kee M Tung
Primary Examiner
Art Unit 2671